

Abstract

5 A circuit for control of an output current in a multiple unit cell array includes an array of unit cells arranged in rows and columns. Each unit cell includes a column select transistor being adapted for control by a column selector and a row select transistor being adapted for control by a row selector. The column select transistor and the row select transistor are connected together in series to each other and between an output node and a first supply. A return electrode is provided to complete the circuit.

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